

## ABSTRACT OF THE DISCLOSURE

A method for fabricating improved integrated circuit devices. The method enables selective hardening of gate oxide layers and includes providing a semiconductor substrate having a gate oxide layer formed thereover. A resist is then formed over the gate oxide layer and patterned to expose one or more areas of the gate oxide layer which are to be hardened. The exposed portions of the gate oxide layer are then hardened using a true remote plasma nitridation (RPN) scheme or a high-density plasma (HDP) RPN scheme. Because the RPN scheme used in the method of the present invention runs at low temperature, the patterned resist remains stable through the RPN process, and those areas of gate oxide layer which are exposed by the patterned resist are selectively hardened by the RPN treatment, while those areas covered by the patterned resist remain unaffected.